TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOS III)

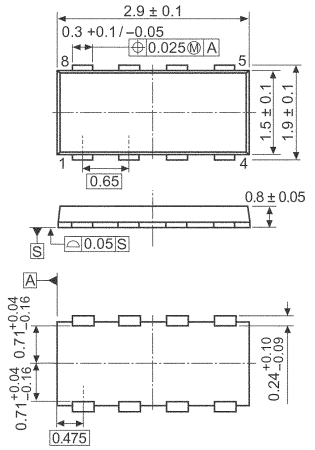
# TPCF8301

Notebook PC Applications

Portable Equipment Applications

- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 72 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 4.7 S (typ.)
- Low leakage current: $I_{DSS}$ = −10 μA (max) ($V_{DS}$ = −20 V)
- Enhancement model: $V_{th}$ = −0.5 to −1.2 V
  ($V_{DS}$ = −10 V, $I_D$ = −200 μA)

Unit: mm



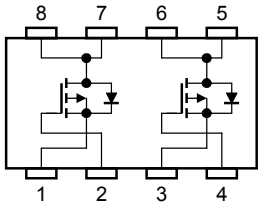

| | |
|---|---|
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-3U1B |

Weight: 0.011 g (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | −20 | V |
| Drain-gate voltage ($R_{GS}$ = 20 kΩ) | | $V_{DGR}$ | −20 | V |
| Gate-source voltage | | $V_{GSS}$ | ±8 | V |
| Drain current | DC (Note 1) | $I_D$ | −2.7 | A |
| | Pulse (Note 1) | $I_{DP}$ | −10.8 | |
| Drain power dissipation (t = 5 s) (Note 2a) | Single-device operation (Note 3a) | $P_{D\ (1)}$ | 1.35 | W |
| | Single-device value at dual operation (Note 3b) | $P_{D\ (2)}$ | 1.12 | |
| Drain power dissipation (t = 5 s) (Note 2b) | Single-device operation (Note 3a) | $P_{D\ (1)}$ | 0.53 | |
| | Single-device value at dual operation (Note 3b) | $P_{D\ (2)}$ | 0.33 | |
| Single pulse avalanche energy (Note 4) | | $E_{AS}$ | 1.2 | mJ |
| Avalanche current | | $I_{AR}$ | −1.35 | A |
| Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5) | | $E_{AR}$ | 0.11 | mJ |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55~150 | °C |

## Circuit Configuration




Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

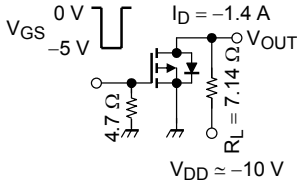
## Thermal Characteristics

| Characteristics | | Symbol | Max | Unit |
|---|---|---|---|---|
| Thermal resistance, channel to ambient (t = 5 s) (Note 2a) | Single-device operation (Note 3a) | $R_{th\ (ch\text{-}a)\ (1)}$ | 92.6 | °C/W |
| | Single-device value at dual operation (Note 3b) | $R_{th\ (ch\text{-}a)\ (2)}$ | 111.6 | |
| Thermal resistance, channel to ambient (t = 5 s) (Note 2b) | Single-device operation (Note 3a) | $R_{th\ (ch\text{-}a)\ (1)}$ | 235.8 | °C/W |
| | Single-device value at dual operation (Note 3b) | $R_{th\ (ch\text{-}a)\ (2)}$ | 378.8 | |

Note: (Note 1), (Note 2), (Note 3), (Note 4), (Note 5) and (Note 6): See the next page.

This transistor is an electrostatic-sensitive device. Please handle with caution.

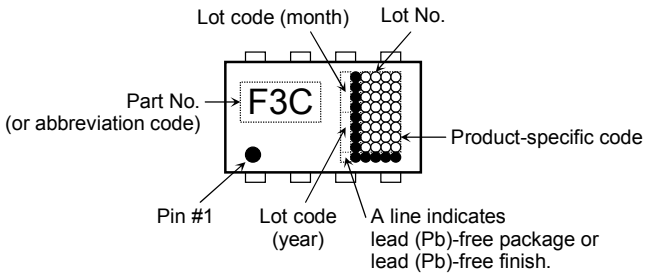
## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V | — | — | ±10 | μA |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = −20 V, $V_{GS}$ = 0 V | — | — | −10 | μA |
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = −10 mA, $V_{GS}$ = 0 V | −20 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = −10 mA, $V_{GS}$ = 8 V | −12 | — | — | |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = −10 V, $I_D$ = −200 μA | −0.5 | — | −1.2 | V |
| Drain-source ON resistance | | $R_{DS\ (ON)}$ | $V_{GS}$ = −1.8 V, $I_D$ = −0.7 A | — | 215 | 300 | mΩ |
| | | $R_{DS\ (ON)}$ | $V_{GS}$ = −2.5 V, $I_D$ = −1.4 A | — | 110 | 160 | |
| | | $R_{DS\ (ON)}$ | $V_{GS}$ = −4.5 V, $I_D$ = −1.4 A | — | 72 | 110 | |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = −10 V, $I_D$ = −1.4 A | 2.4 | 4.7 | — | S |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = −10 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 470 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 70 | — | |
| Output capacitance | | $C_{oss}$ | | — | 80 | — | |
| Switching time | Rise time | $t_r$ |   Duty ≦ 1%, $t_w$ = 10 μs | — | 5 | — | ns |
| | Turn-on time | $t_{on}$ | | — | 9 | — | |
| | Fall time | $t_f$ | | — | 8 | — | |
| | Turn-off time | $t_{off}$ | | — | 26 | — | |
| Total gate charge (gate-source plus gate-drain) | | $Q_g$ | $V_{DD}$ ≃ −16 V, $V_{GS}$ = −5 V, $I_D$ = −2.7 A | — | 6 | — | nC |
| Gate-source charge | | $Q_{gs}$ | | — | 4 | — | |
| Gate-drain (“miller”) charge | | $Q_{gd}$ | | — | 2 | — | |

## Source-Drain Ratings and Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain reverse current | Pulse (Note 1) | $I_{DRP}$ | — | — | — | −10.8 | A |
| Forward voltage (diode) | | $V_{DSF}$ | $I_{DR}$ = −2.7 A, $V_{GS}$ = 0 V | — | — | 1.2 | V |

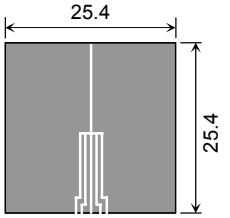
## Marking (Note 6)




Note 1: Ensure that the channel temperature does not exceed 150°C.

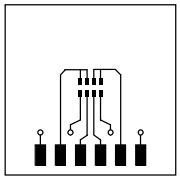
Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)

Note 3: a) The power dissipation and thermal resistance values are shown for a single device




FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(a)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(b)

(During single-device operation, power is only applied to one device.).

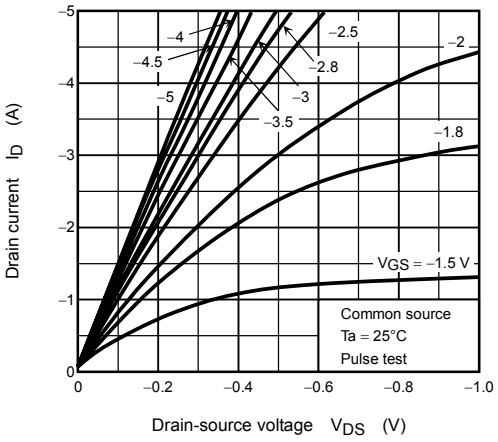
b) The power dissipation and thermal resistance values are shown for a single device
(During dual operation, power is evenly applied to both devices.).

Note 4: $V_{DD}$ = −16 V, $T_{ch}$ = 25°C (initial), L = 0.5 mH, $R_G$ = 25 Ω, $I_{AR}$ = −1.35 A

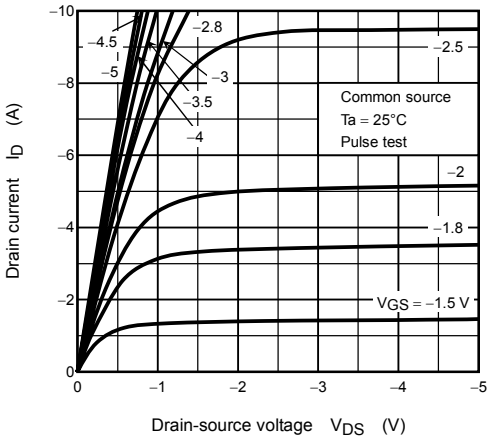
Note 5: Repetitive rating: Pulse width limited by maximum channel temperature.

Note 6: A dot on the lower left of the marking indicates Pin 1

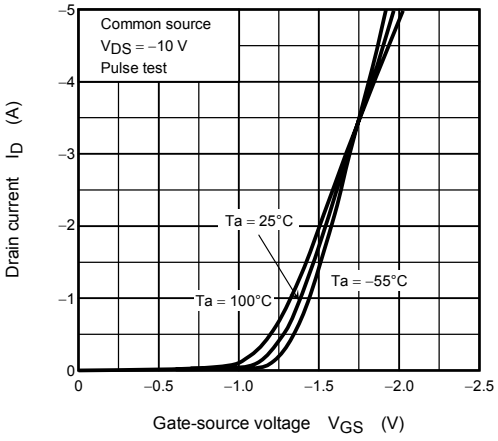
$I_D - V_{DS}$



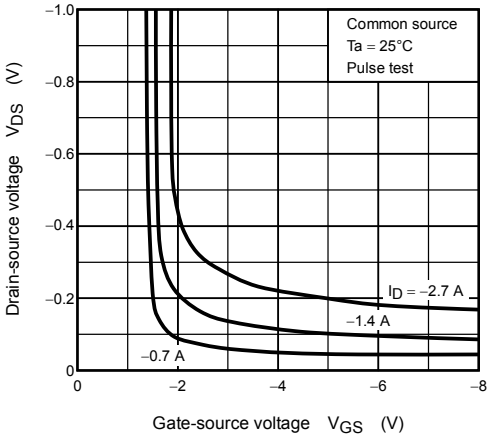

$I_D - V_{DS}$



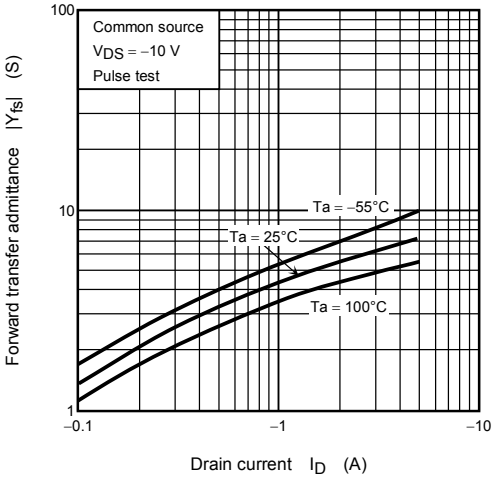

$I_D - V_{GS}$



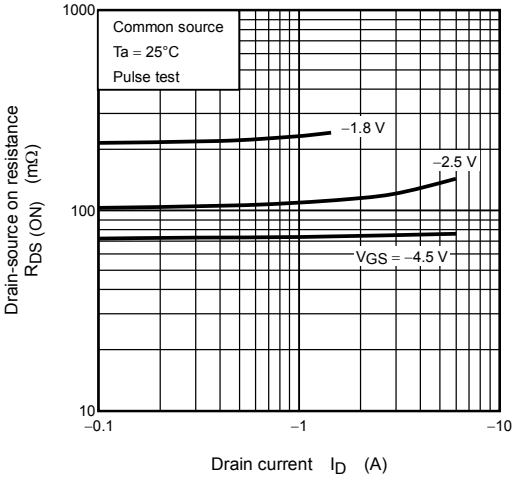

$V_{DS} - V_{GS}$



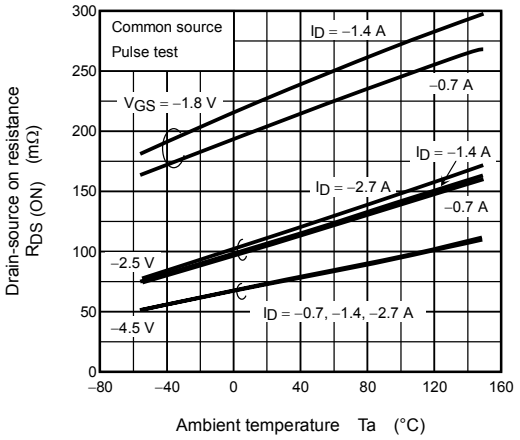

$|Y_{fs}| - I_D$



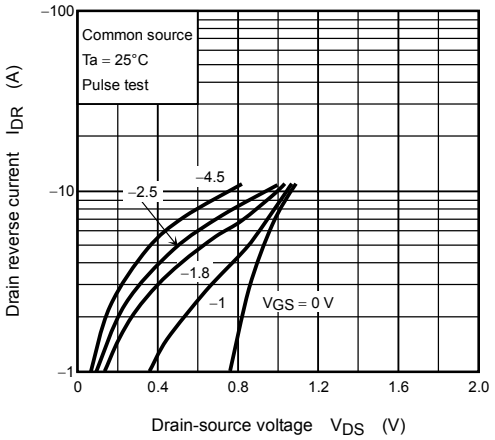

$R_{DS\ (ON)} - I_D$



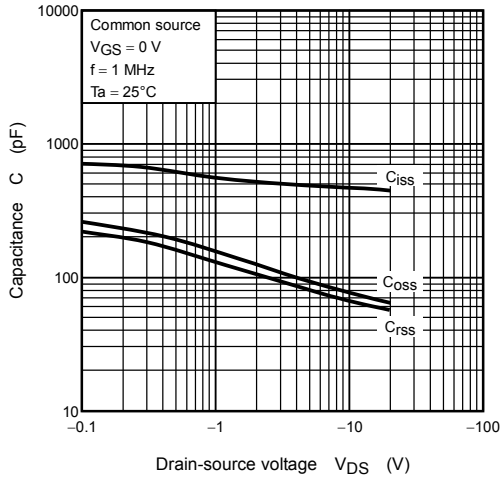
$R_{DS\ (ON)}$ – Ta



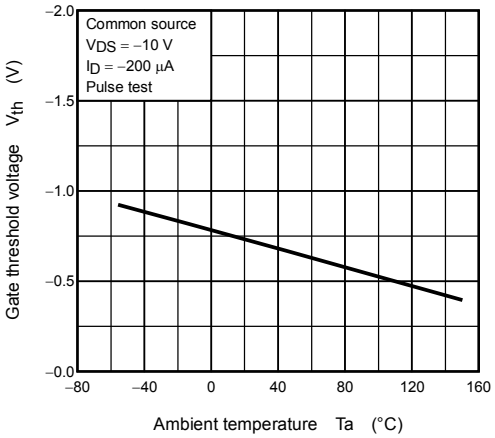

$I_{DR}$ – $V_{DS}$



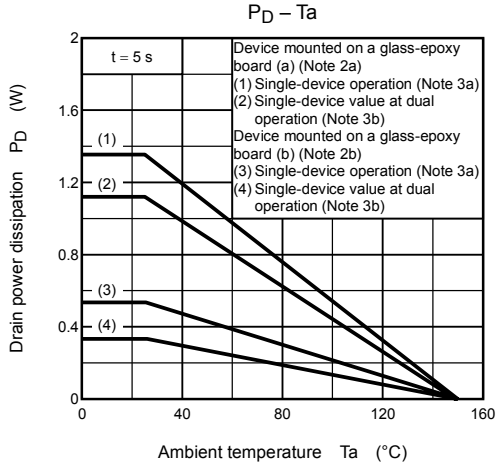

Capacitance – $V_{DS}$



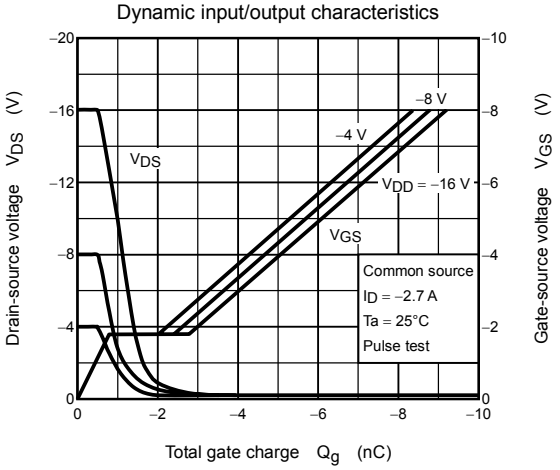

$V_{th}$ – Ta

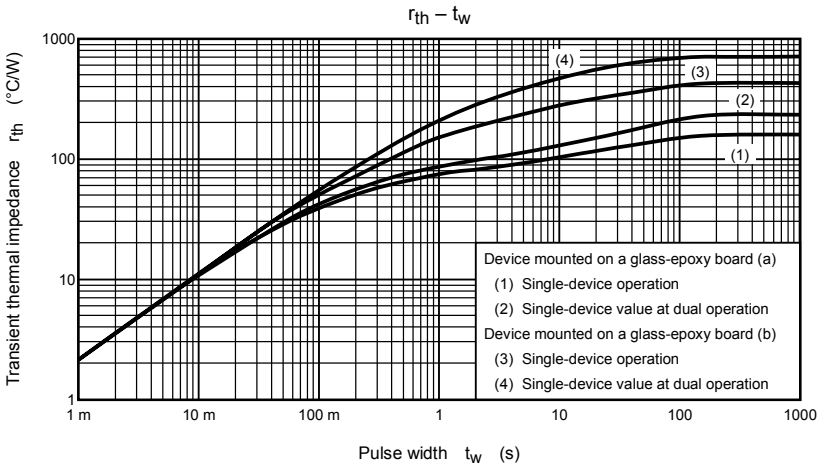


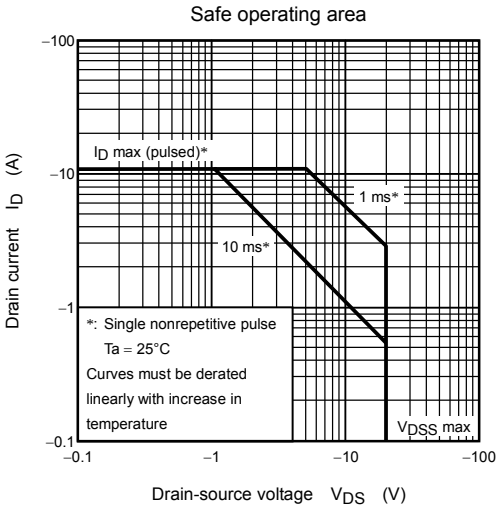

$P_D$ – Ta




Dynamic input/output characteristics




$r_{th} - t_w$
Transient thermal impedance $r_{th}$ (°C/W)
1000
100
10
1
1 m
10 m
100 m
1
10
100
1000
Pulse width $t_w$ (s)
(4)
(3)
(2)
(1)
Device mounted on a glass-epoxy board (a)
(1) Single-device operation
(2) Single-device value at dual operation
Device mounted on a glass-epoxy board (b)
(3) Single-device operation
(4) Single-device value at dual operation


Safe operating area
Drain current $I_D$ (A)
−100
−10
−1
−0.1
$I_D$ max (pulsed)*
1 ms*
10 ms*
*: Single nonrepetitive pulse
Ta = 25°C
Curves must be derated
linearly with increase in
temperature
$V_{DSS}$ max
−0.1
−1
−10
−100
Drain-source voltage $V_{DS}$ (V)

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